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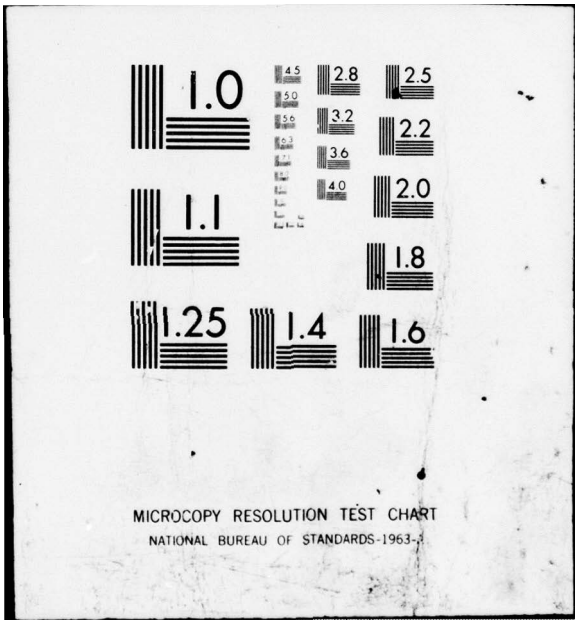
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MONOLITHIC 20W 2GHz TRANSISTOR AND MONOLITHIC 5W 4GHz TRANSISTOR

QUARTERLY REPORT NO. 6

14 SEPTEMBER 1978 - 13 DECEMBER 1978

CONTRACT NO. DAAB07-77-C-0431

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ELECTRONICS MATERIEL READINESS COMMAND
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This project has been accomplished as part of the U. S. Army (Manufacturing the Technology) Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

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Via
V-groove
Buffered Epi

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A lot of L-10 devices was fabricated and provided 8 watts in saturation, only 1dB less than the contract goal. A new passivation process was developed to provide an excellent etch mask against hydrazine.

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TABLE OF CONTENTS

		PAGE NO.
SECTION I	INTRODUCTION	1
SECTION II	TECHNICAL WORK THIS QUARTER	3
2.0	INTRODUCTION	3
2.1	POST VIA PROCESS	3
2.1.1	Si_3N_4 PASSIVATION	3
2.1.2	SILOX PROCESS	4
2.2	L-10 DEVICE RESULTS	5
2.2.1	DC TEST RESULTS	5
2.2.2	RESISTANCE TESTS	7
SECTION III	CONCLUSIONS	11
SECTION IV	PROGRAM FOR THE NEXT INTERVAL	13
SECTION V	PUBLICATIONS, REPORTS, AND CONFERENCES	15
SECTION VI	IDENTIFICATION OF PERSONNEL	17

LIST OF TABLES

TABLE I.	DC BREAKDOWN VOLTAGES	6

LIST OF ILLUSTRATIONS

Figure 1.	L-10 Internal Resistances	8

SECTION I

INTRODUCTION

During this period of work, the post via process was implemented to provide a via on the L-10 device.

The L-10 devices produced fell only 1dB short of the output power goal. The loss of power was due to excessive collector series resistance.

No text on this page.

SECTION II

TECHNICAL WORK THIS QUARTER

2.0 INTRODUCTION

The post via process was used to fabricate a wafer of L-10 devices. Plasma deposited Si_3N_4 was used as the passivant, but it failed to protect the major portion of the wafers processed. An improved Silox passivation scheme has been developed to provide better protection during the via etch process.

2.1 POST VIA PROCESS

2.1.1 Si_cN_v Passivation

Si_3N_4 films from three different vendors were evaluated on test wafers. The films appeared to cover the metallized wafers in an acceptable manner as deposited. However, several wafers began to show cracking of the films several days after deposition. Virtually every wafer showed failure of the films after the wet chemistry fabrication steps of photoresist removal after contact opening. Plasma stripping of the photoresist was used to reduce the film failure on subsequent wafers.

The failures of these films indicate a very stressed system. The Si_3N_4 was found to flake off in large pieces over large metal areas such as bonding pads and feeder bars.

There is no actual chemical bond between the Si_3N_4 and gold, the only adhesion mechanism is mechanical, and the stresses in these films are apparently sufficient to overcome the mechanical adhesion.

This is also true of Silox to even a greater extent. However, Silox is known to produce an aluminum-oxygen bond when deposited on aluminum conductors, and, consequently, Silox sticks to aluminum quite well.

2.1.2 Silox Process

It would not be feasible to change the L-10 metal system to aluminum to enhance Silox adhesion; however, we have developed a process to obtain the reliability of a gold metal system with the passivation adhesion of an aluminum system.

This is done by depositing a thin layer aluminum on top of the gold metallization and heat treating the wafers until a stable intermetallic is formed. Bonding pads and feeder bars, where second layer metal or wire bonds are to contact, are protected by a patterned layer of photoresist. The aluminum deposited on those areas is removed by lifting off the photoresist. Aluminum, silicon, and gold do not occur in the same physical locations so that purple plague is not formed.

The Silox is then deposited and has been found to stick

so well it cannot be scratched off. The films survive heat treatment and both dry and wet chemistry. Most important, the Silox film will successfully mask the active device against the 100°C hydrazine used as the via etch.

Several wafers of L-10 devices are in the process of via fabrication using this technique.

2.2 L-10 DEVICE RESULTS

A wafer of L-10 devices was fabricated by the post via process using Si_3N_4 as a passivant. This was the only wafer of several on which there were areas in which the Si_3N_4 did not fail. The overall yield on the wafer was three dice.

Aluminum was used as the ohmic contact metal in the vias. The vias provided an ohmic contact to the substrate.

2.2.1 DC Test Results

Data was taken on the dice from the one wafer to characterize breakdown voltage and internal resistances.

The breakdown voltage data is shown in Table I.

TABLE I

dc BREAKDOWN VOLTAGES

S/N	H_{fe} 5V 100mA	BV_{ceo} 10mA	BV CES 10mA	BV CBO 10mA	BV_{ebo} 10mA
1	25	60	60	60	4.9
2	10	37	52	52	5.1
3	18	40	54	54	4.9

2.2.2. Resistance Tests

The L-10 device has three resistive structures which are external to the active transistor. These are the via resistance, the top contact collector resistance and the emitter ballast resistance. These three resistors are shown in Figure 1.

The emitter ballast resistance was found to be very close to the design target, but the via resistance and collector resistance were found to be much higher than desired.

The vias on this lot used aluminum as the ohmic contact metal. Ohmic contacts were formed to the P+ substrate; however, the via resistance was found to be 0.35Ω per via, at least six times the desired value. This was caused by two factors, excessive substrate resistivity and excessive substrate thickness.

The desired substrate resistivity is 0.005Ω-cm; however, the epi vendor insisted on using higher resistivity substrates, 0.014Ω-cm, to control autodoping during the growth of the intrinsic layer. The substrates were also thicker than desired because the back lap process was prematurely terminated to prevent damage to the vias. The vias on this particular wafer had flat bottoms due to poor alignment of the via patterns to the crystalographic planes, which resulted in severe undercutting of the via mask during via etch. The etch was terminated when the vias were 3.4 mils deep, leaving the flat bottoms in the vias. Previous experience with flat bottom vias indicated that the flat bottoms of

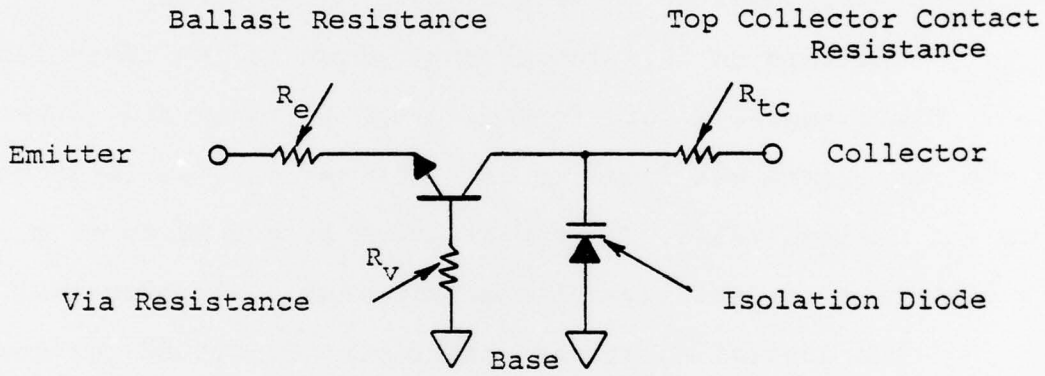

Figure 1. L-10 Internal Resistances

such vias would break through during back lapping if the wafer was lapped to less than 1 mil from the via bottom. This wafer was lapped to within 1.1 mil of the via bottom. Normal vias which are etched to completion can be lapped to within 0.2 mil from the via bottom before damage will occur.

The extra silicon, and the higher resistivity of the silicon under the via, can account for a factor of six increase in via resistance.

The collector series resistance is higher than desired on this lot due mostly to high resistivity and thickness of the N^- epi layer. The high resistivity N- layer manifested itself in two ways. First, the devices produced optimum power output at much too high an operating voltage. The intended operating voltage for these devices is 28V; however, this wafer performed best at a voltage of 40V. Also, the junction capacitance is lower than expected, also indicating high resistivity.

Measurements of the resistivity of <100> silicon on the SRP (spreading resistance probe) have proven to be inaccurate due to the lack of adequate resistivity standards for <100> silicon.

The result of the high N^- resistivity was reduced saturated power. The output power of the devices was 8.1W CW at 2GHz, an improvement over the last lot, but still about 1dB below specification. Power gain was 4.6dB at a collector efficiency of 25.3%. At 1GHz the RF performance was greatly improved. A

maximum of 17.5W CW was obtained with 9.7dB gain and 46.5% efficiency. The 1GHz performance is favorably comparable with that of other typical 2GHz designs.

SECTION III.

CONCLUSIONS

The L-10 devices produced to date nearly meet the required performance specifications. The yield has been low due to process difficulties which have been solved. More L-10 devices are nearly complete and will yield much better and should perform better, also.

No text on this page.

SECTION IV.

PROGRAM FOR THE NEXT INTERVAL

The passivation problem on the L-10 devices absorbed about four months engineering effort and has yet to be fully proven on active L-10 devices. L-10 devices using the Silox passivation will be fabricated during the next quarter. The excessive collector resistance will probably exist on future wafers from the same epitaxial runs as the wafers already processed.

The in-house epitaxial reactor is on-line and is being certified for the production of epitaxial material of better quality than has been obtained from outside vendors. Initial tests indicate that the intrinsic material grown in our system exceeds 800Ω-cm, which is at least twice the value required. Also, the correct substrate material will be used and the N^+ buried layer will be the correct resistivity and thickness. The N^- layer will also be deposited somewhat thinner than the existing material to reduce the collector resistance further.

When these changes in the epitaxy are made, we feel that the performance of the L-10 will exceed the contract specifications and be comparable to state-of-the-art chip-and-wire devices.

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SECTION V.

PUBLICATIONS, REPORTS, AND CONFERENCES

There were no publicatons or conferences during this quarter.

Monthly Report Nos. 16, 17, and 18 were submitted during this reporting period.

No text on this page.

SECTION VI IDENTIFICATION OF PERSONNEL

	Hours
Joseph Courier	177
Alan Harrington	270
Robert Jenkins	270
James Scheppele	124
George Schreyer	93
George Skelly	177
Frank Bartel	89
Harold Bjornson	74
Dorothy May	85
Norman Nissen	73
Eugenia Nunez	70
Lois Reed	83
Stephanie Wesche	85
William Imhauser	175
Ken Kam	72
Chet Winham	79
Antonio Morawski	75
Anne Bayard	74
Arthur Durschlag	73
Carl Bridges	73
Ruth Moore	83
Robert Etchells	67
Kim Tarrant	57
Donald Stauder	41
Andrew Marchette	81
Evelyn Jeffers	83
C. Delgado	70
Richard Allison	25
Leon Jostad	55

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